Introduction to
NetFPGA
And
OpenFlow
Outline

• NetFPGA
  - FPGA
  - Programming on an FPGA
  - NetFPGA

• OpenFlow
  - OpenFlow Protocol
  - OpenFlow Switch

• OpenFlow Switch using NetFPGA
  - Switch Structure
  - Switch Demo
NetFPGA
FPGA

- **Field-programmable Gate Array (FPGA)** is an integrated circuit designed to be configured after manufacturing.
- The configuration is specified using a hardware description language (HDL), e.g., Verilog.
- FPGAs contain logic blocks which generally can be arbitrarily connected together.
- FPGAs can be used to implement any logical function that an ASIC (an integrated circuit customized for a particular use) could perform.
Programming on an FPGA

- Specification
- High Level Design
- Micro Design/Low level design
- RTL Coding Simulation
- Synthesis
- Place & Route
- Post Silicon Validation
NetFPGA - 1G

• A reconfigurable hardware platform for 1Gbps high-speed networking.

• Components
  - Processor: Xilinx Virtex-II Pro 50 FPGA.
  - Memory:
    (1) 4.5 MB SRAM for storing tables.
    (2) 64 MB DDR2 DRAM for buffering packets.
  - Gigabit Ethernet Ports: 4 x 1 Gbps bi-directional Ethernet ports.
NetFPGA - 1G contd.

- Components
  - Multi-gigabit I/O: 2 SATA connectors for chaining multiple NetFPGAs.
  - standard PCI: Compatible with a PCI-X slot.
  - Hardware Debugging port.
Figure 2: Detailed block diagram of the components of the NetFPGA board.
NetFPGA - 10G

- Coming soon...
Questions?
OpenFlow
OpenFlow Protocol

- Modern Ethernet switches and routers contain flow-tables that run at line-rate to implement firewalls, NAT, QoS, and to collect statistics.
- OpenFlow is an open protocol for modifying the flow-table in different switches and routers.
- OpenFlow allows the control paths to be outside the switches or routers.
OpenFlow Protocol contd.

- Definition of a flow
- 12-tuple

<table>
<thead>
<tr>
<th>Ingress Port</th>
<th>Ether source</th>
<th>Ether dst</th>
<th>Ether type</th>
<th>VLAN id</th>
<th>VLAN priority</th>
<th>IP src</th>
<th>IP dst</th>
<th>IP proto</th>
<th>IP ToS bits</th>
<th>TCP/UDP src port</th>
<th>TCP/UDP dst port</th>
</tr>
</thead>
</table>

Table 2: Fields from packets used to match against flow entries.
OpenFlow Switch

- A switching device is an OpenFlow Switch if (1) it has a flow table which performs packet lookup and forwarding. (2) it has a secure channel to an external controller which is in charge of configuring the flow table in (1).

- An entry in the flow table

| Header Fields | Counters | Actions |

Header Fields are fields in the flow definition.
OpenFlow Switch contd.
OpenFlow Switch contd.

- Workflow for an OpenFlow Switch
  a packet arrives
  look up the packet in the flow table
  if there is a match
    take the corresponding action
  else
    send the packet to the controller
  do what the controller decide to do
  (adding a new flow for the packet is optional)
OpenFlow Switch contd.

Figure 1: Steps when a new flow arrives at an OpenFlow switch.
OpenFlow Switch using NetFPGA
Switch Structure

OpenFlow Controller

OpenFlow Protocol (SSL/TCP)

Control Path

OpenFlow

Data Path (Hardware)
Switch Structure contd.

![Diagram of Switch Structure]

- Input Arbiter
- Header Parser
- Wildcard Lookup
- Exact Match Lookup
- Arbiter
- Packet Editor
- OpenFlow Output Port Lookup
- User Data Path
- SRAM
- DRAM
- Output Queues
Switch Demo
Initialization

- Load the router circuit into the FPGA on the NetFPGA.
- Setup the datapath for the OpenFlow Switch.
- Setup the OpenFlow Controller.
- Setup the OpenFlow protocol stack for the OpenFlow Switch and connect to the OpenFlow Controller.
Scenario 1

- 2 senders and 1 receiver in a Y-shape topology. Sender 1: 192.168.2.202 --> port1 on NetFPGA
  Sender 2: 192.168.2.203 --> port2 on NetFPGA
  Receiver: 192.168.2.201 --> port3 on NetFPGA

- The controller does NOTHING. This scenario is for purely demonstrating how the flow table works on the NetFPGA.

- Use **dpctl** to manually configure the flow table.
Scenario 2

- 2 senders and 1 receiver in a Y-shape topology. 
  Sender 1: 192.168.2.202 --> port1 on NetFPGA 
  Sender 2: 192.168.2.203 --> port2 on NetFPGA 
  Receiver: 192.168.2.201 --> port3 on NetFPGA 

- The OpenFlow Switch acts as a learning switch.
Questions?
The End